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The Variables and Invariants in the Evolution of Logic Optical Lithography Process

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Abstract: Photolithography has been a major enabler for the continuous shrink of the semiconductor manufacturing design rules. Throughout the years of the development of the photolithography, many new technologies have been invented and successfully implemented, such as image projection lithography, chemically amplified photoresist, phase shifting mask, optical proximity modeling and correction, etc. From 0.25 μm technology to the current 7 nm technology, the linewidth has been shrunk from 250 nm to about 20 nm, or 12.5 times. Although imaging resolution is proportional to the illumination wavelength, with the new technologies, the wavelength has only been shrunk from 248 nm to 134.7 nm (193 nm immersion in water), less than 2 times. Would it mean that the imaging performance has been continuously declining? Or we have yet fully utilized the potential of the photolithography technology? In this paper, we will present a study on the key parameters and process window performance of the image projection photolithography from 0.25 μm node to the current 7 nm node.

Keywords: image projection photolithography, imaging contrast, exposure latitude, mask error factor, linewidth uniformity, chemically amplified photoresist, phase shifting mask, optical proximity correction, and photoacid diffusion length.

1. Introduction

Image projection photolithography has replaced contact/proximity printing for better resolution and defect consideration. The earliest projection exposure tools are developed by David A. Markler and Abe Offner from Perkin-Elmer company [1–2], where an all reflective 1:1 imaging system has been adopted. It has been found that the use of a ring field can cancel aberration and make good imaging. This system can offer a numerical aperture (NA) of 0.33, a ring field of 3 inch diameter, 1 mm width. The imaging resolution is 2 μm with 5.5 μm depth of focus and +/-1 μm overlay. Its illumination uniformity is +/-10% and distortion is +/- 1 μm. The system takes minimally 6 seconds for 1 wafer exposure. The advantage of all reflective design is that the alignment and exposure wavelengths can share the same optics and there is no chromatic aberration. But the limitation is numerical aperture and it cannot correct all aberration with just a few reflective surfaces. Later, partially refractive or all refractive designs that adopted double gauss, double telecentric designs have been used for more advanced design rules [3-4].

From the photoresist side, starting in the 1970's, the i-line (365 nm) or g-line (436 nm) photoresist Diazonaphthoquinone (DNQ)/Novolac [5] has been widely used for 5 μm to 0.25 μm. At 0.25 μm technology, the higher resolution and more efficient chemically amplified photoresist (CAR) based on Poly-hydroxystyrene (PHOST) has emerged [6-7]. The chemically amplified photoresist contains a photoacid generator (PAG), such as Triphenylsulfonium trifluoromethyl sulfonate, which will disassociate and create a strong acid under UV exposure. The hydrogen ion will catalyze polymer deprotection reaction and make the deprotected polymer to dissolve in aqueous developer. Unlike the photosensitive component in the DNQ/Novolac photoresist, the photoactive compound (PAC), the photoacid can diffuse and trigger 15-30 deprotection reactions, which improves the efficiency of photochemical reaction by more than an order of magnitude. Of course the diffusion of the photoacid molecules will reduce image contrast and it must be controlled.

Throughout the years in the developing of suitable photolithography process for processes from 0.25 μm to the current 7 nm technology nodes, we have worked with various type exposure tools and chemically amplified photoresists. Also equipped with a constant threshold simulation tool with Gaussian diffusion (to simulate photoacid diffusion

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length in the CAR), we systematically studied the parameters in the photolithography and found the invariants in the process, the imaging contrast and CDU related mask error factor (MEF).

2. Technologies that have been Invented and Implemented in the Photolithography

Photolithography has been the critical and most complex technology in the integrated circuit industry. For the simple task of replicate circuit designs with high efficiency and good quality, numerous new tools, materials, devices, or methods/methodologies have been invented and put to quick use. Figure 1 has listed the major invented tools, materials, devices, or methods/methodologies in several categories, namely the exposure tools, the photoresist/anti-reflection coatings, the photomask, the process/wafer track/etch process, the optical proximity correction, and the design rules.

In Figure 2, the technology nodes where the above mentioned inventions are used is displayed. For example, the quadrupole illumination mode is first used in the 90 nm logic technology node, the polarization in the illumination is first used in the 45 nm technology node, the opaque Molybdenum-Silicide on glass (OMOG) mask was first used in the 22 nm technology node, etc. In the figure, there are some technology that are superseded by more advanced version, such as, the rule-based optical proximity correction (OPC) has been used in 0.25 and 0.18 μm technologies, but was replaced by more advanced model-based OPC starting 0.13 μm technologies. The wafer CDU tuning within dose mapping methodology (DoMa) that are used in 0.13 μm technology was replaced by more advanced dose mapping and correction within both exposure shot and wafer version starting the 90 nm technology node. There is also some special technology that have only been used in several technology modes. One of them is the alternating phase shifting mask (Alt-PSM) that has been used for 3 technology nodes.

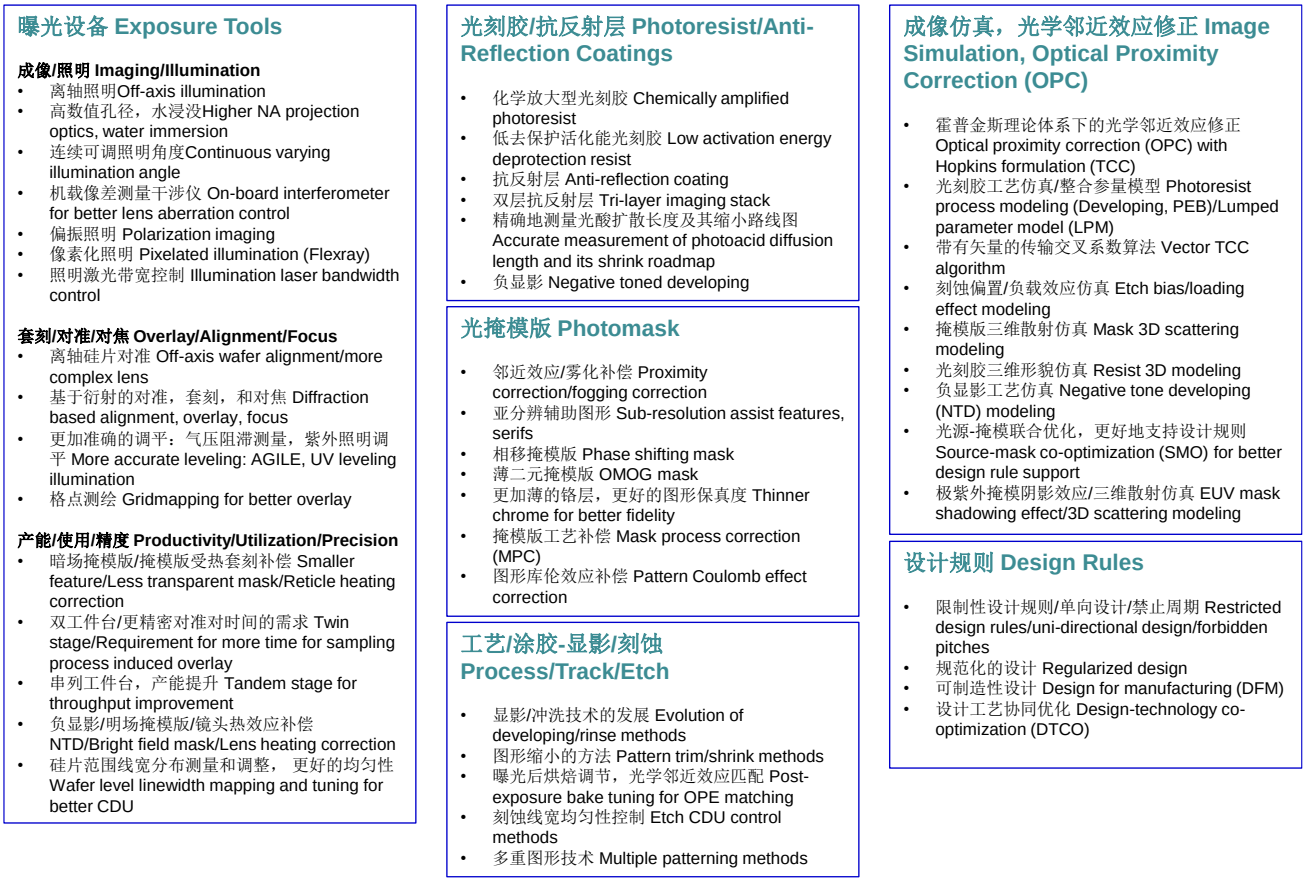

Figure 1. Invented tools, materials, devices, or methods/methodologies for photolithography.

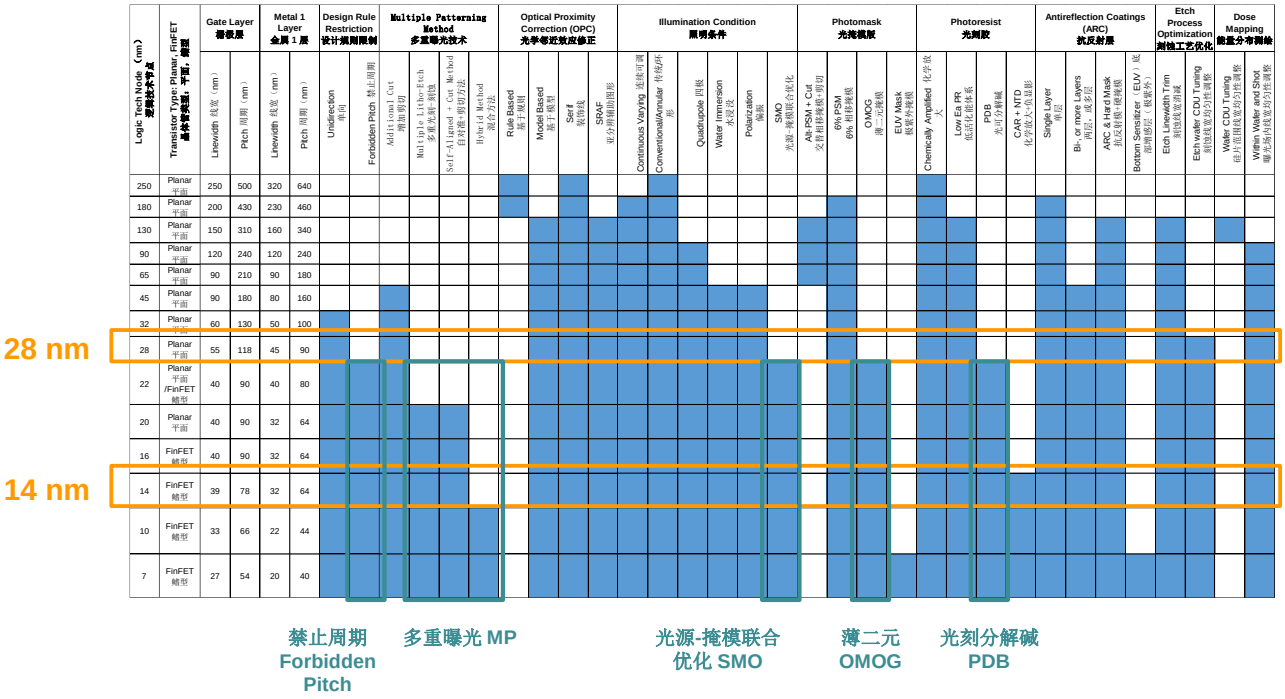

Figure 2. Invented tools, materials, devices, or methods/methodologies for photolithography and the technology nodes where they are used.

3. Major Process Parameters by Logic Technology Nodes

The most common parameters that characterizes photolithography process are as follows:

- Exposure latitude/Depth of focus (EL/DoF)
- Photoresist etch resistance/thickness/thickness uniformity
- Photoresist cross section profile
- Across chip/across wafer linewidth variation (ACLV/AWLV)
- Pattern corner rounding

Over the years, more parameters have been added:

- CD through pitch (~1999, 180 nm node)
- Forbidden pitch (2002, 110 nm node)
- Mask error factor (2002, 110 nm node)
- Linewidth roughness, line edge roughness (~2003, 90 nm node)
- OPC matching (~2005, 65 nm node)
- Tip to tip separation (2007, 45 nm node)
- Circularity (~2007, 45 nm node)
- Immersion defectivity (2007, 45 nm node)
- Corner rounding (2011, 28 nm node)
- NTD optical proximity deviation from optical model (2015, 14 nm node)

The addition is a result of increasingly higher requirement for process window and linewidth uniformity and the need to be able to fully model and utilize the process. For example, the CD through pitch is introduced due to increasingly small k1 value under which only isolated to dense linewidth bias cannot describe the optical proximity effect well. When the proximity effect becomes more pronounced, there is certain pitch range can become very difficult to print. The “forbidden pitch” was used to describe this effect starting around 110 nm process nodes. Although the so-called “forbidden pitch” is not really avoided by design until nodes below 28 nm, the device patterns designed within such pitch range does have degraded linewidth uniformity performance. The mask error factor (MEF) has become a severe issue at the 110 nm technology node. In the years of 65 nm node, the 193 nm dry process has reached a limit, the optical proximity effect has become challenging, and the understanding of 193 nm photoresist has become mature [8-9], there emerges a need to match OPC from different photoresist and exposure tools to speed up process transfer and expansion. In the years of the 45 nm technology node, the tip-to-tip separation has become a limitation for the chip design, the 193 nm immersion photoresist can print a tip-to-tip distance around 60-70 nm, which is close to the CD of 80-90 nm. At more advanced technology nodes, the tip-to-

tip distance will not improve much, the limit of the parameter is 55 nm for positive toned developing (PTD) and 60 nm for negative toned developing (NTD). However, at the most advanced technology nodes 7 nm, the metal CD is around 20 nm through double patterning, significantly smaller than the above tip-to-tip distance (55-60 nm) that the 193 nm immersion process can support.

Circularity is a parameter that measures the pattern fidelity of contact/via hole printing. When the overlay becomes critical, it can affect total yield. However, the circularity is just like linewidth roughness (LWR) or line edge roughness (LER), which is very difficult to improve. Usually the limit of LWR is 4 nm (3-sigma), which is a reflection of photoresist granularity and image contrast and can only be realized using dipole illumination and low activation energy photoresist. For the contact layer, the only illumination that is practical is annular. A sensible LWR range is around 6-8 nm. In case of overlay issue, it would be better to improve OPC accuracy and CDU rather than focusing on the circularity improvement.

Immersion defectivity has emerged with the introduction of 193 nm water immersion photolithographic process. Although it seems to mostly attribute to the hardware improvement, the photoresist has also been required to leach less into the immersion water.

Corner rounding is basically ignored before the introduction of 32/28 nm technology nodes. The corner rounding radius for the 248 nm process is around 100-160 nm, and 35-45 nm for the 193 nm immersion process. At the 32/28 nm technology nodes, the corner rounding radius has approached the CD numbers, which are 45-50 nm for 193 nm immersion layers and 145-160 nm for the 248 nm layers. Small corner rounding radius can help to shrink chip area.

NTD process has been introduced at 14 nm MEOL and BEOL layers, it has the advantages of superior contrast and MEF performance for the semi-dense and isolated pitches. And even for the dense pitch, its performance has been improving to the minimally acceptable level. NTD process, however is not friendly to the OPC modeling. Its linewidth can differ from the traditional PTD model by 15-20 nm at semi-dense and isolated pitches. Until very recently, it has been understood [10]. The NTD process, similar to that of most negative toned photoresist, relies on some level of saturation in the photochemical reaction. The saturation process is non-linear and will deviate from the original linear representation of the aerial image from the photoacid diffusion-reaction process. For a successful process development, the similarity of a NTD process to the linear optical model is important to cycle time and CDU.

4. Major Process Window Values by Logic Technology Nodes

Shown in Figures 4(a) and 4(b) is a table of important process window parameter values for various technology nodes from 0.25 μm to 7 nm. The parameters list here is the exposure latitude (EL) and mask error factor (MEF). The numbers here are simulated with typical process parameters, such as the mask type (binary, 6% attenuated phase shifting, OMOG), photoresist thickness, pitch, linewidth, wavelength (248 nm, 193 nm, 193 nm immersion), photoacid diffusion length (from 70 to 5 nm), the illumination condition (conventional, annular, cross quadrupole, weak dipole, strong dipole, SMO). The figures show that the illumination condition evolves from the conventional and annular used by 0.25 μm through 65 nm, to dipole and quadrupole used to 45 nm through 22 nm, and to pixelated (source-mask optimized, SMO'ed) used by 20 nm through 7 nm. The evolution of the illumination condition reflects the need to print ever smaller pitch. At the same time, the wavelength has also been reduced from 248 nm to about 134.7 nm, though not much. There is another important parameter that shrinks aggressively: the photoacid diffusion length. It has been reduced from the 70 nm at the 0.25 μm technology node to about 5 nm at 22 nm and below nodes, a 14 time shrink. This has been mostly overlooked by many lithographers. But the magnitude of the shrink has demonstrated itself to be at the same level to that of the linewidth (around 12.5 X from 250 nm to 20 nm).

Shown in Figures 5(a) and 5(b) are exposure latitude numbers for the gate and metal 1 layers at the minimum pitch for the technology nodes ranging from 0.25 μm to 7 nm. The data indicates that the exposure latitude for the gate layer is basically constant, at 18% or above, with the exception of 78 nm pitch at 14 nm node (where the gate line is mostly connection wire). The metal layer, however, has an exposure latitude going from an initial high number of 28% at 0.25 μm technology node and gradually decreasing and remain constant at 65 nm nodes. The constant is around 13%. The 18% and 13% numbers are a result of linewidth uniformity

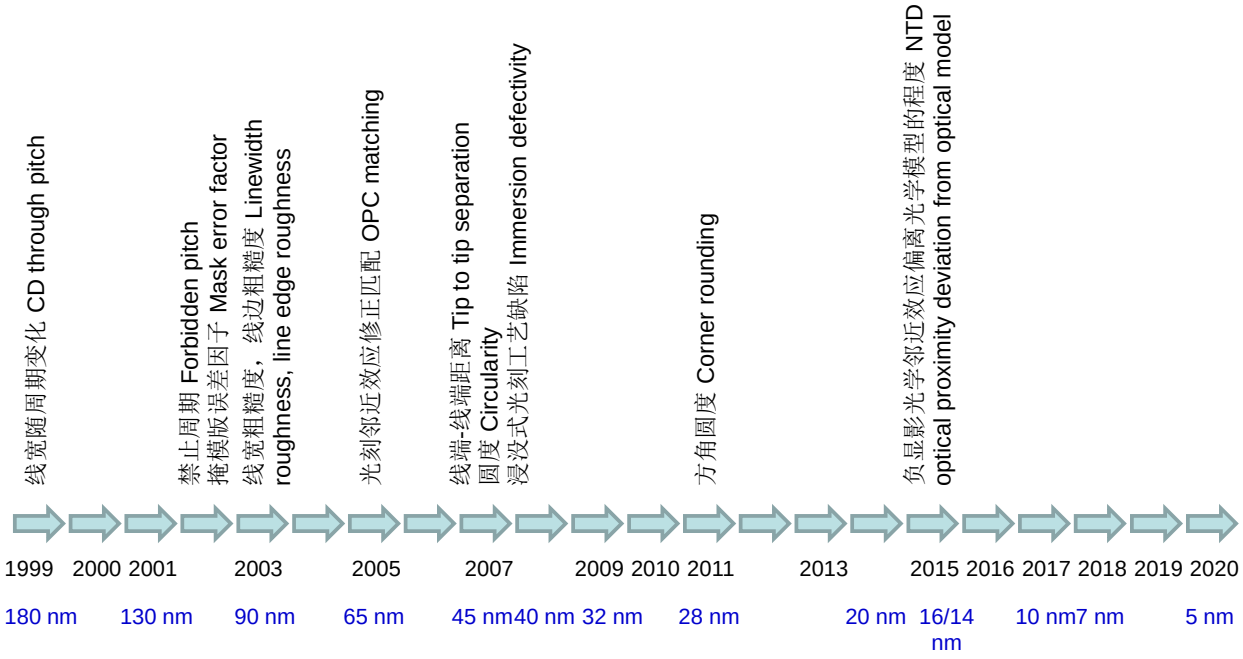

Figure 3. The year and technology node when some photolithographic process parameters have been added.

Logic Tech Node（nm） 逻辑技术节点	Transistor Type: Planar, FinFET 晶体管类型：平面，鳍型	Gate Layer 栅极层									Metal 1 Layer 金属 1 层									
		Mask：Binary/6% PSM/OMOG 掩模版：二元/6% 相移/薄二元	Photoresist Thickness（nm） 光刻胶厚度（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Wavelength（nm）/Polarization 波长（nm）/偏振	Photoacid Diffusion Length（nm） 光酸扩散长度（nm）	Illumination Condition 照明条件	Exposure Latitude (EL) 曝光宽容度	Mask Error Factor (MEF) 掩模版误差因子	Trench/Line 沟槽/线条	Mask：Binary/6% PSM/OMOG 掩模版：二元/6% 相移/薄二元	Photoresist Thickness（nm） 光刻胶厚度（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Wavelength（nm）/Polarization 波长（nm）/偏振	Photoacid Diffusion Length（nm） 光酸扩散长度（nm）	Illumination Condition 照明条件	Exposure Latitude (EL) 曝光宽容度	Mask Error Factor (MEF) 掩模版误差因子
250	Planar 平面	Binary 二元	700	250	500	248	70	0.55NA/Conventional 传统	19.3	1.47	Line 线条	Binary 二元	1000	320	640	248	70	0.55NA/Conventional 传统	29.3	1.03
180	Planar 平面	6% PSM 6% 相移	500	180	430	248	60	0.65NA/Annular 环形	17.7	1.39	Line 线条	6% PSM 6% 相移	600	230	460	248	70	0.60NA/Annular 环形	18.1	1.85
130	Planar 平面	6% PSM 6% 相移	400	150	310	248	30	0.70NA/Annular 环形	18.9	1.66	Trench （Copper）沟槽 （铜线引入）	6% PSM 6% 相移	400	160	340	248	30	0.70NA/Annular 环形	19.8	1.69
90	Planar 平面	6% PSM 6% 相移	300	120	240	193	25	0.70NA/Annular 环形	19.7	1.56	Trench 沟槽	6% PSM 6% 相移	300	120	240	193	30	0.70NA/Annular 环形	16.9	2
65	Planar 平面	6% PSM 6% 相移	220	90	210	193	20	0.85NA/Annular 环形	18.6	1.51	Trench 沟槽	6% PSM 6% 相移	200	90	180	193	20	0.75NA/Annular 环形	13.4	2.85
45	Planar 平面	6% PSM 6% 相移	200	90	180	193 immersion /XY pol 浸没/XY偏振	15	1.1NA/Annular 环形	22.5	1.51	Trench 沟槽	6% PSM 6% 相移	180	80	160	193 immersion /XY pol 浸没/XY偏振	15	1.1NA/Annular 环形	14.9	2.63
32	Planar 平面	6% PSM 6% 相移	110	60	130	193 immersion /XY pol 浸没/XY偏振	15	1.25NA/Weak DP 双二极	18.95	1.47	Trench 沟槽	6% PSM 6% 相移	110	50	100	193 immersion /XY pol 浸没/XY偏振	15	1.25NA/CQ 交叉四极	11.9	3.5
28	Planar 平面	6% PSM 6% 相移	110	55	118	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/Weak DP 双二极	21.5	1.4	Trench 沟槽	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/CQ 交叉四极	12.6	3.2
22	Planar 平面 /FinFET 鳍型	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 双二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	OMOG 薄二元	70	40	80	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 双二极/光源-掩模联合优化	8.9 (with PDB含PIB：12.7)	3.5
20	Planar 平面	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 双二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	6% PSM 6% 相移	90	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	12.6 (Pitch周期=90)	3.2 (Pitch周期=90)
16	FinFET 鳍型	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 双二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	6% PSM 6% 相移	90	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	12.6 (Pitch周期=90)	3.2 (Pitch周期=90)
14	FinFET 鳍型	OMOG 薄二元	70	39	78/84	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Strong DP/SMO 双二极/光源-掩模联合优化	13.7/23.1	2.8/1.47	Line-NTD 线条-负显影	6% PSM 6% 相移	70	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	9.63 (with PDB含PIB：13.98) （Pitch周期=90）	3.58 (Pitch周期=90)
10	FinFET 鳍型	6% PSM6% 相移	70	33	66 （SADP+Cut+LE） 自对准双重+剪切+单次	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 双二极/光源-掩模联合优化	16.2/24.3 (Pitch周期=90/132)	3.1/1.1 (Pitch周期=90/132)	Line-NTD 线条-负显影	6% PSM 6% 相移	70	22	44（LESLE+Cut） 自对准辅助二重光刻刻蚀	193 immersion /XY pol 浸没/XY偏振	7	1.35NA/Weak DP/SMO 双二极/光源-掩模联合优化	12.55 (Pitch周期=88)	3.35 (Pitch周期=88)
7	FinFET 鳍型	6% PSM 6% 相移	70	27	54 (SADP+Cut+LE) 自对准双重+剪切+单次	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 双二极/光源-掩模联合优化	19.9/25.4 (Pitch周期=90/108)	2.3/1.22 (Pitch周期=90/108)	Trench 沟槽	OMOG 薄二元	70	20	40（LE2,SE Pitch=80）二重光刻刻蚀，单次光刻周期=80	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 双二极/光源-掩模联合优化	8.9 (with PDB含PIB：12.7) (Pitch周期=80)	3.5 (Pitch周期=80)

(a)

Logic Tech Node（nm） 逻辑技术节点	Transistor Type: Planar, FinFET 晶体管类型：平面，鳍型	Gate Layer 栅极层									Metal 1 Layer 金属 1 层									
		Mask: Binary/6% PSM/OMOG 掩模版：二元/6% 相移/单二元	Photoresist Thickness（nm） 光刻胶厚度（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Wavelength（nm）/Polarization 波长（nm）/偏振	Photoacid Diffusion Length（nm） 光酸扩散长度（nm）	Illumination Condition 照明条件	Exposure Latitude (EL) 曝光能量宽容度	Mask Error Factor (MEF) 掩模版误差因子	Trench/Line 沟槽/线条	Mask: Binary/6% PSM/OMOG 掩模版：二元/6% 相移/单二元	Photoresist Thickness（nm） 光刻胶厚度（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Wavelength（nm）/Polarization 波长（nm）/偏振	Photoacid Diffusion Length（nm） 光酸扩散长度（nm）	Illumination Condition 照明条件	Exposure Latitude (EL) 曝光能量宽容度	Mask Error Factor (MEF) 掩模版误差因子
250	Planar 平面	Binary 二元	700	250	500	248	70	0.55NA/Conventional 传统	19.3	1.47	Line 线条	Binary 二元	1000	320	640	248	70	0.55NA/Conventional 传统	29.3	1.03
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20	Planar 平面	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	6% PSM 6% 相移	90	32	64（LE2，SE Pitch=90：二重光刻/刻蚀，单次光刻周期=90）	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	12.6 (Pitch周期=90)	3.2 (Pitch周期=90)
16	FinFET 鳍型	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	6% PSM 6% 相移	90	32	64（LE2，SE Pitch=90：二重光刻/刻蚀，单次光刻周期=90）	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	12.6 (Pitch周期=90)	3.2 (Pitch周期=90)
14	FinFET 鳍型	OMOG 薄二元	70	39	78/84	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Strong DP/SMO 强二极/光源-掩模联合优化	13.7/23.1	2.8/1.47	Line-NTD 线条-负显影	6% PSM 6% 相移	70	32	64（LE2，SE Pitch=90：二重光刻/刻蚀，单次光刻周期=90）	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	8.63 (with PDB 含ITO，13.98) （Pitch周期=90）	3.58 (Pitch周期=90)
10	FinFET 鳍型	6% PSM/6%	70	33	66 （SADP+Cut+LE：自对准双重+剪切+单次	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	16.2/24.3 (Pitch周期=90/132)	3.1/1.1 (Pitch周期=90/132)	Line-NTD 线条-负显影	6% PSM 6% 相移	70	22	44（LESLE+Cut：自对准侧墙二重光刻/刻蚀	193 immersion /XY pol 浸没/XY偏振	7	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	12.55 (Pitch周期=88)	3.35 (Pitch周期=88)
7	FinFET 鳍型	6% PSM 6% 相移	70	27	54 (SADP+Cut+LE) 自对准双重+剪切+单次	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	19.9/25.4 (Pitch周期=90/108)	2.3/1.22 (Pitch周期=90/108)	Trench 沟槽	OMOG 薄二元	70	20	40（LE2,SE Pitch=80）二重光刻/刻蚀，单次光刻周期=80	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	8.9 (with PDB 含ITO，12.7) (Pitch周期=80)	3.5 (Pitch周期=80)

传统/环形 Conventional /Annular

四极/二极 Quadrupole /Dipole

像素化Pixelated（SMO）

- 照明条件从传统/环形照明，逐渐发展为四极、二极、像素化（SMO）。 The exposure condition has been evolving from the conventional/annular gradually to quadrupoles, dipoles, and pixelated （SMO）

(b)

Figure 4. (a) A simulated EL and MEF numbers for the Gate and Metal layers for typical technology nodes from 0.25 μm to the 7 nm. (b) Same to (a) with categorization.

requirement. To make this more intuitive, we correlate the exposure latitude numbers with imaging contrast.

Shown in Figures 5(a) and 5(b) are exposure latitude numbers for the gate and metal 1 layers at the minimum pitch for the technology nodes ranging from 0.25 μm to 7 nm. The data indicates that the exposure latitude for the gate layer is basically constant, at 18% or above, with the exception of 78 nm pitch at 14 nm node (where the gate line is mostly connection wire). The metal layer, however, has an exposure latitude going from an initial high number of 28% at 0.25 μm technology node and gradually decreasing and remain constant at 65 nm nodes. The constant is around 13%. The 18% and 13% numbers are a result of linewidth uniformity requirement. To make this more intuitive, we correlate the exposure latitude numbers with imaging contrast.

Described in Figure 6 is a schematic illustrating the definition of exposure latitude. At the minimum pitch, the aerial image of a dense line/space is a sinusoidal function due to interference of two light beams (the zeroth order and the first order). Noticing the definition of the image contrast, defined in Equation (1), the aerial image intensity $U(x)$ can be written in the form shown in Equation (2), as follows,

$$contrast = \frac{U_{max} - U_{min}}{U_{max} + U_{min}} \tag{1}$$

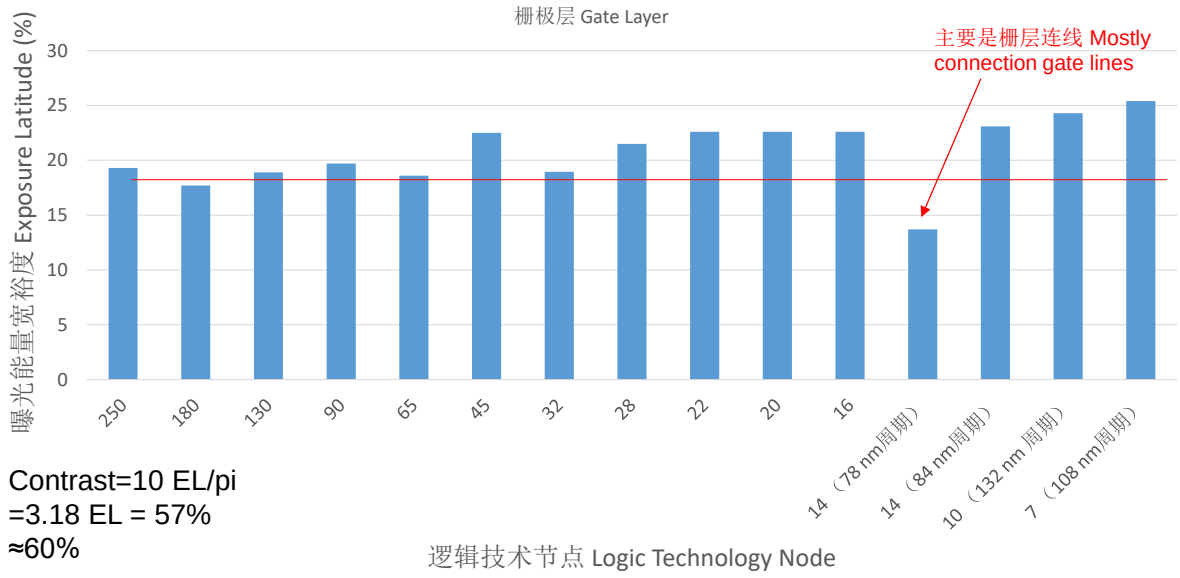
$$\begin{aligned} U(x) &= \frac{(U_{max} + U_{min})}{2} + \frac{(U_{max} - U_{min})}{2} cos\left(\frac{2\pi x}{p}\right) \\ &= U_0\left(1 + contrast\ cos\left(\frac{2\pi x}{p}\right)\right) \end{aligned} \tag{2}$$

where U_{max} and U_{min} represents the maximum and minimum intensity, respectively, p represents pitch and U_0 is a proportional constant.

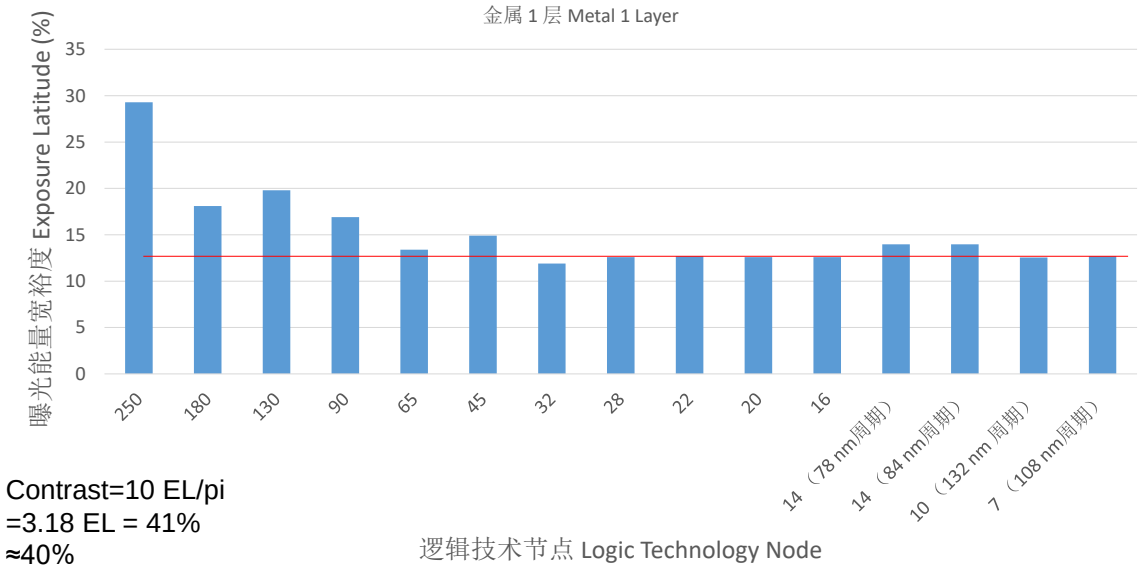
The definition of the exposure latitude EL is the ratio of the exposure energy spread to the exposure energy to linewidth target ΔE due to +/- 10% linewidth variation, defined in Equation (3), as follows,

$$EL = \frac{\Delta E\left(corresponding\ to \pm 10\%\ linewidth\right)}{E} \tag{3}$$

$$\begin{aligned} EL &= \frac{\Delta E\left(corresponding\ to \pm 10\%\ linewidth\right)}{E} \\ &= \frac{1}{U_0}\left|\frac{dU(x)}{dx}\right| \Delta L = contrast\ \frac{2\pi}{p} \sin\left(\frac{2\pi L}{p}\right) \Delta L \end{aligned} \tag{4}$$



(a)



(b)

Figure 5. (a) A simulated EL for the Gate layer as a function of technology nodes from 0.25 μm to the 7 nm. (b) A simulated EL for the Metal layer as a function of technology nodes from 0.25 μm to the 7 nm..

According to Equation (2), Equation (3) can be written as Equation (4), where L and ΔL represent linewidth and linewidth variation range, which is $0.1L$. When the linewidth L equals to the 1/2 of the pitch p, Equation (4) can be simplified as follows,

$$EL = contrast \frac{\Delta L}{L} \pi = \frac{\pi}{10} contrast, \quad \text{or} \quad contrast = \frac{L}{\Delta L} \frac{EL}{\pi} = \frac{10}{\pi} EL \tag{5}$$

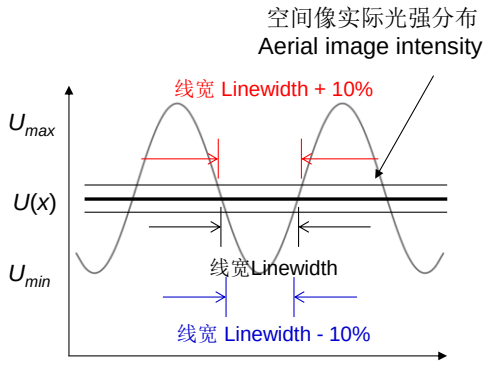
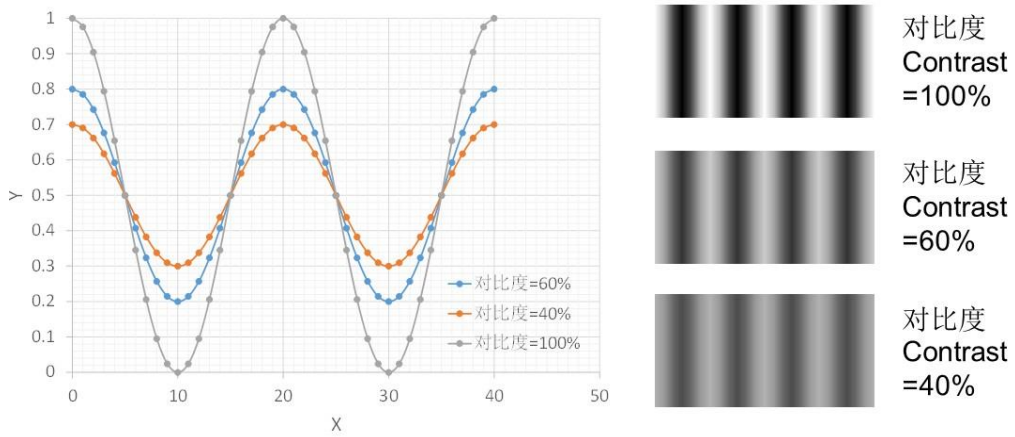


Figure 6. Schematic that illustrates the definition of exposure latitude

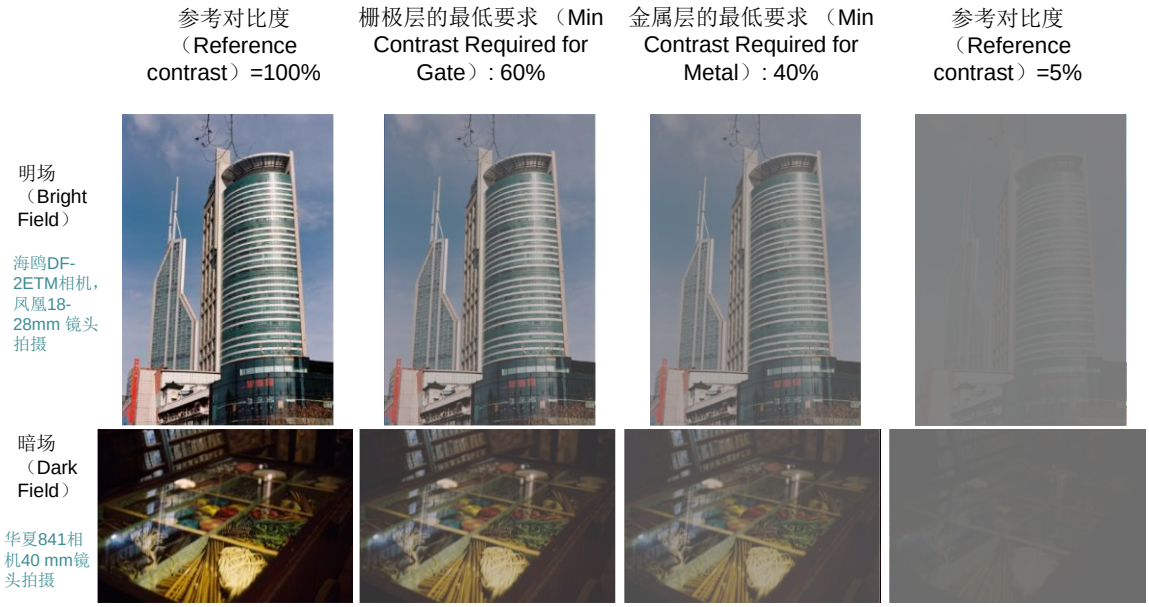
According to Equation (5), the imaging contrast is roughly 3.2 *EL*. Therefore the 18% and 13% exposure latitude for the dense pitches are equivalent to image contrast numbers of 57.6% and 41.6%, respectively, or roughly 60% and 40%.

Shown in Figures 7(a) are simulated 1D line/space grey scale images at three level of image contrast: 100%, 60%, and 40%, respectively. The images indicate that the needed gate layer contrast is visibly better than that of the metal layer. Shown in Figure 7(b) are two photos under bright field and dark field conditions showing the same three level of image contrast plus a 5% contrast for comparison. The 40% contrast images seems to reach a comfortable-uncomfortable limit while the 60% contrast images seems to reveal all image details with just a casual glance (my feeling, laugh). These are the analogy to the everyday photography.

The other important parameter of the process window we will show is the mask error factor (MEF), or the so-called mask error enhancement factor (MEEF). If the exposure latitude is related to image contrast, which is related to the across wafer linewidth uniformity, the mask error factor will be related to the within exposure shot linewidth uniformity.

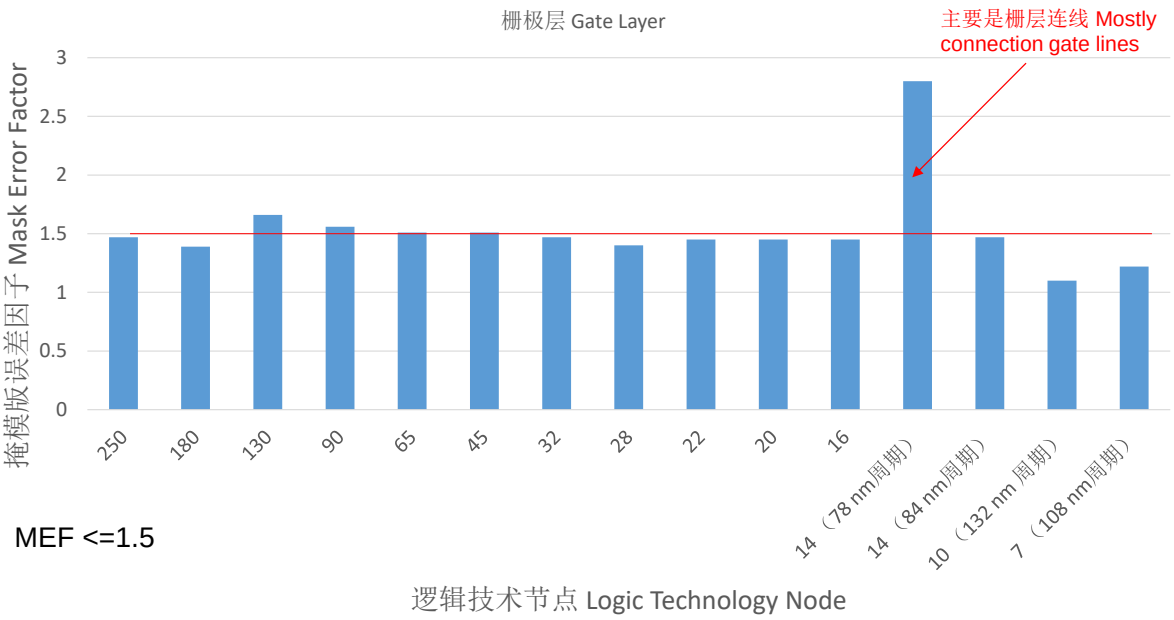


(a)

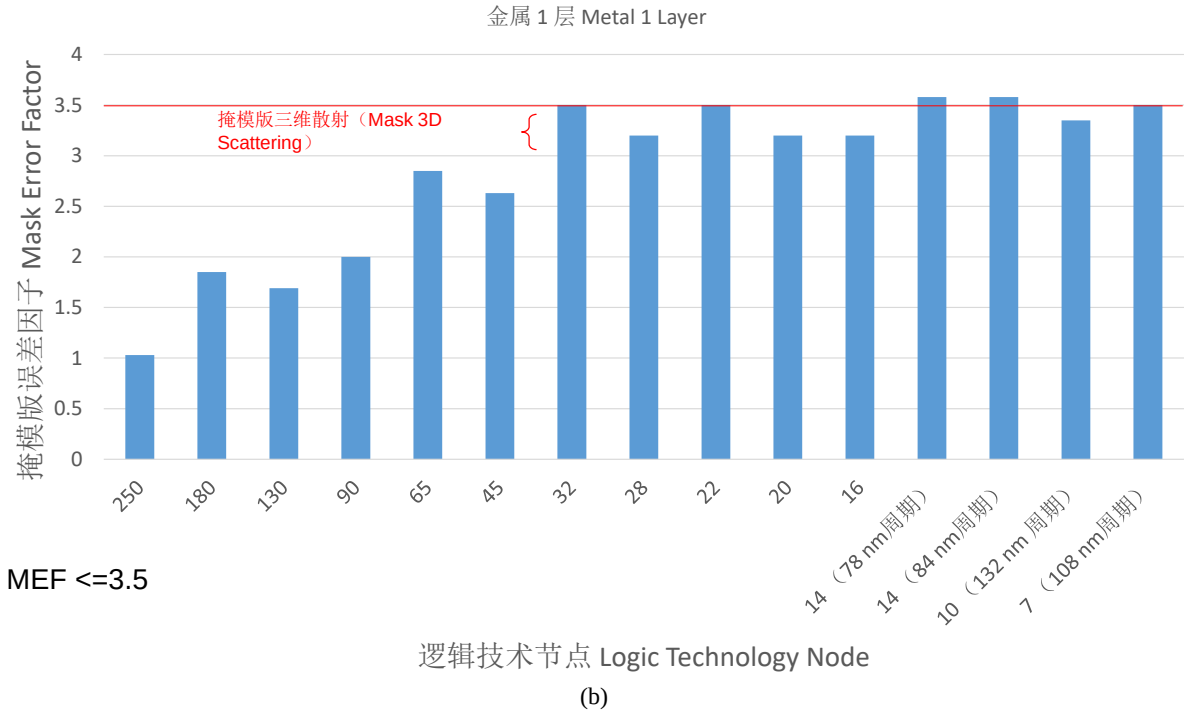


(b)

Figure 7. (a) Plots of 1D line/space images showing 3 level of image contrasts: 100%, 60%, and 40%, respectively. (b) Photos of both bright field and dark field types at 4 level of image contrasts: 100%, 60%, r40%, and 5%, respectively.



(a)



(b)

Figure 8. (a) A simulated MEF for the Gate layer as a function of technology nodes from 0.25 μm to the 7 nm. (b) A simulated MEF for the Metal layer as a function of technology nodes from 0.25 μm to the 7 nm.

Figures 8(a) and 8(b) show mask error factor numbers for the gate and metal 1 layers at the minimum pitch for the technology nodes ranging from 0.25 μm to 7 nm. As we can see, the MEF for the gate layer remains pretty much as 1.5 or lower with the exception of 78 nm pitch at 14 nm node (where the gate line is mostly connection wire). And the MEF for the metal layer starts at an initial low number of 1 at the 0.25 μm technology node and gradually increasing and remain constant at 32 nm nodes. The constant is around 3.5. A small jump at the 32 nm technology node is due to the mask 3D scattering effect, which adds about 0.7 on top of the 45 nm MEF values. The 3.5 versus 1.5 indicates that the metal linewidth uniformity can have a relaxed tolerance compared to the gate.

5. Linewidth Uniformity Requirement by Logic Technology Nodes

As a continuation from the last section, in this section we summarize our study of linewidth uniformity requirement for different technology nodes. We starts from the ITRS (International Technology Roadmap for Semiconductors) publication on the recommended numbers [11-13]. Shown in Table 1 is a list of ITRS pitch/CD number and CD uniformity (CDU) requirement for technology nodes from 130 nm to 5 nm. We reference three ITRS publication versions: the ITRS 2001, 2005, and 2013. In case of any difference between the versions, we pick the more recent numbers. In the last two lines of the Table 1, we calculate the ratios of the CDU to both the gate physical CD and gate half pitch.

The calculation reveals the following:

(1) The gate linewidth control tolerance relative to its physical linewidth is nearly constant, about +/- 10%.

(2) The gate linewidth control tolerance relative to gate half pitch increases as the *diffraction limit is approached* (20 nm and 16/14 nm nodes) from +/- 3% to +/- 4%, and to +/-5% as *double patterning methods are used* (10 nm, 7 nm, and 5 nm nodes).

The above result reflects that the key to the gate linewidth uniformity control is to support CMOS transistor performance requirement which follows a fixed linewidth uniformity requirement during the course of design rule shrink. And the physical linewidth becomes closer to the half pitch.

Accordingly, the mask linewidth uniformity has also followed a trend of reduction as the technology nodes advance. Shown in Table 2 is a list of mask linewidth uniformity specification originally from the ITRS 2001, 2005, and 2013, and adjusted with the practical mask making capabilities for the gate layer. The top 3 lines below the line of technology nodes are 4X specifications, and the next 3 lower lines are 1X specifications (4X number divided by 4), and the next lower 3 lines are wafer total CDU numbers (also from Table 1), the last 3 lines are the ratio of mask linewidth uniformity multiplied by MEF numbers to the total CDU numbers, which shows a trend going from 0.52 at the 130 nm node to a low 0.38 at the 20 nm node and rises to a 0.48 at the 5 nm node. This number is nearly constant.

Figures 9 shows the ratio of mask linewidth uniformity for both the gate and metal layers multiplied by MEF to the total wafer CDU as a function of technology nodes from 130nm to the 5 nm. As discussed before, the gate MEF is nearly constant at 1.5, the ratio of mask CDU contribution (mask CDU multiplied by MEF) to the total wafer CDU is also nearly constant at 0.4-0.5. This means that the mask contribution to the total wafer CDU for the gate is kept at about 0.4-0.5. In the case of the metal layer, however, the situation is different. Starting from 130 nm through 45 nm, the contribution from the mask is quite low, around 0.20 to about 0.30, from 32 nm node and newer, the contribution from the mask is similar to that of the gate layer, around 0.4-0.5. This is because a jump in MEF about 0.70 due to the mask 3D scattering effect.

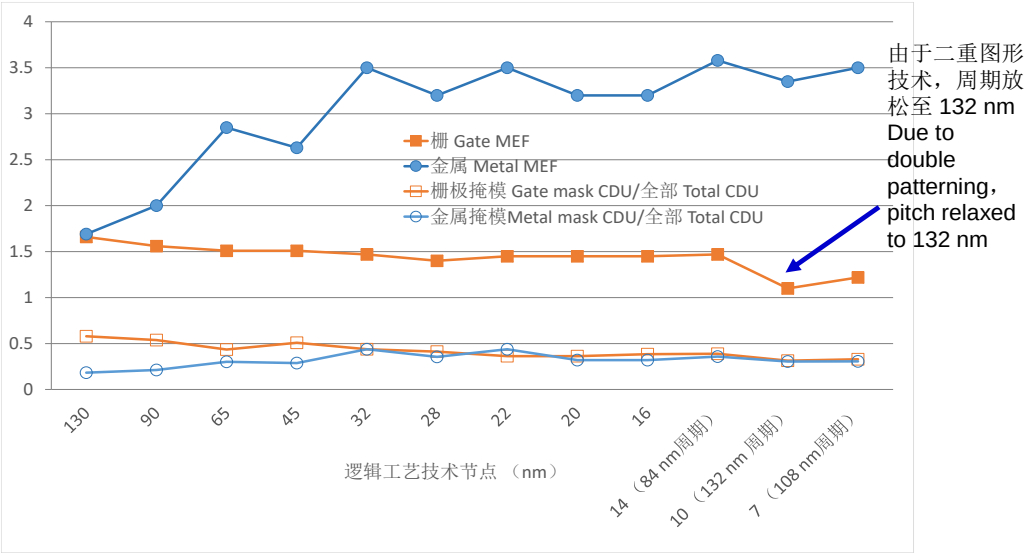


Figure 9. Ratio of mask linewidth uniformity for both the gate and metal layers multiplied by MEF to the total wafer CDU as a function of technology nodes from 130nm to the 5 nm. And the MEF values for both the gate and metal layers multiplied by MEF to the total wafer CDU as a function of technology nodes from 130nm to the 5 nm.

Table 1. CDU requirement for the gate layer at major logic technology nodes.

生产年代 Year of Production	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
逻辑工艺技术节点 Logic Technology Node (nm)	**130**		**90**		**65**		**45**	**40**	**32**		**28**			**20**	**16/14**		**10**	**7**		**5**
逻辑半周期 Logic Half Pitch (ITRS2001)	150	130	107	90	80	70	65													
逻辑金属半周期 Logic Metal Half Pitch (ITRS2005)					90	78	68	59	52	45	40	36	32							
逻辑金属半周期 Logic Metal Half Pitch (ITRS2013)													40	32	32	28	25	23	20	18
逻辑代工半周期-金属1层 Foundry Half Pitch-Metal 1 (nm)	170		120		90		80	60	50		45			32	32		22	20		16
逻辑代工半周期-栅极 Foundry Half Pitch-Gate (nm)	155		120		105		90	81	65		59			45	43.5		33	27		22
栅极物理线宽 Gate Physical CD (nm) ITRS 2001	65		45		32		25													
栅极物理线宽 Gate Physical CD (nm) ITRS 2005					32		25	23	20		16		13							
栅极物理线宽 Gate Physical CD (nm) ITRS 2013													20	18	17		14	13		11
线宽均匀性 CDU (3sigma,nm) ITRS 2001	5.3		3.7		2.6		2													
线宽均匀性 CDU (3sigma,nm) ITRS 2005					3.3		2.6	2.3	2.1		1.7		1.3							
线宽均匀性 CDU (3sigma,nm) ITRS 2013													2	1.8	1.7		1.4	1.3		1.1
线宽均匀性/栅极物理线宽 CDU/Gate Physical CD (%)	8.2%		8.2%		10.3%		10.4%	10.0%	10.5%		10.6%			10.0%	10.0%		10.0%	10.0%		10.0%
线宽均匀性/栅极半周期 CDU/Gate Half Pitch (%)	3.4%		3.1%		3.1%		2.9%	2.8%	3.2%		2.9%			4.0%	3.9%		4.2%	4.8%		5.0%

Table 2. CDU requirement for photomasks at major logic technology nodes.

生产年代 Year of Production	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
逻辑工艺技术节点 Logic Technology Node (nm)	**130**		**90**		**65**		**45**	**40**	**32**		**28**			**20**	**16/14**		**10**	**7**		**5 非极紫外 (Non-EUV)**
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2001 (Binary) (4X)	7.4		5.1		4.2		3.5													
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2005 (4X)					3.8		3.5	3	2.5		2		2							
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2013 (4X)													2	1.8	1.8		1.6	1.6		1.4
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2001 (Binary) (1X)	1.85		1.28		1.05		0.88													
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2005 (1X)					0.95		0.88	0.75	0.63		0.50		0.50							
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2013 (1X)													0.50	0.45	0.45		0.40	0.40		0.35
线宽均匀性 CDU (3sigma,nm) ITRS 2001	5.3		3.7		2.6		2													
线宽均匀性 CDU (3sigma,nm) ITRS 2005					3.3		2.6	2.3	2.1		1.7		1.3							
线宽均匀性 CDU (3sigma,nm) ITRS 2013													2	1.8	1.7		1.4	1.3		1.1
掩模版线宽均匀性*MEF/全部线宽均匀性 Photomask Making CDU*MEF/Total CDU, ITRS 2001	0.52		0.52		0.61		0.66													
掩模版线宽均匀性*MEF/全部线宽均匀性 Photomask Making CDU*MEF/Total CDU, ITRS 2005					0.43		0.50	0.49	0.45		0.44		0.58							
掩模版线宽均匀性*MEF/全部线宽均匀性 Photomask Making CDU*MEF/Total CDU, ITRS 2013													0.38	0.38	0.40		0.43	0.46		0.48

6. Summary of Variables and Invariants

From the above analysis, we conclude for the following:

The Variables:

- Parameters that are used for the photolithographic process evaluation
- Technologies that are used by the photolithographic processes
- The evolving exposure condition from the conventional/annular gradually to quadrupoles, dipoles, and pixelated (SMO)

The Invariants/Nearly Invariants:

- Exposure latitude/Imaging contrast: Gate ≥ 18%, Metal ≥13% [from 0.25 μm to 7 nm]
- Mask error factor (MEF): Gate ≤ 1.5, Metal ≤ 3.5 [from 0.25 μm to 7 nm]
- Gate layer percentage linewidth tolerance relative to physical gate length: +/- 10% [from 130 nm to 5 nm]
- Gate layer percentage linewidth tolerance relative to gate layer half pitch: +/- 3-5% [from 130 nm to 5 nm]
- Mask CDU contribution to the total wafer CDU: 40-50% [from 130 nm to 5 nm]

7. Conclusion

We have done a study on two important photolithography process window parameters, the exposure latitude and mask error factor for technology nodes from 0.25 μm to 7 nm and a linewidth uniformity study from 130 nm to 5 nm technology nodes based on ITRS publication and practical process and equipment capabilities. We have found that although there are many new photolithography tools, materials, devices, or methods/methodologies have been invented and implemented, and there are many new parameters for the characterizing of the photolithographic process, the exposure latitude and mask error factors for the gate and metal layers are either kept constant or have converged to a constant. In the linewidth uniformity study, we have found consistent relative linewidth tolerance in relation to the linewidth targets, e.g., around +/-10% for the physical gate length. We have found that the contribution of the mask CDU to the total wafer CDU is around 40-50%.

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